

REMARKS

By this Response, Applicants propose to amend claims 1, 12, and 24. No claims have been added or further canceled. Claims 6, 9, 11 and 14-23 have been previously canceled. Claims 1-5, 7, 8, 10-13 and 24-33 are pending. Support for the amendments to claims 1, 12 and 24 can be found throughout the as-filed specification and claims, in particular at page 6, lines 15-27. No new matter has been added.

Rejection of Claims 1-5, 7, 8, 10, 12, 13, 24, 25 and 27-33 Under 35 U.S.C. § 102(b)

In the Final Office Action, the Examiner rejected claims 1-5, 7, 8, 10, 12, 13, 24, 25, and 27-33 under 35 U.S.C. § 102(b) as being anticipated by *Ghoshal* (U.S. Patent No. 6,204,165). This rejection is respectfully traversed.

Each of independent claims 1, 12, and 24 is directed to a semiconductor device comprising, *inter alia*, a plurality of substantially non load bearing inter-level dielectric (ILD) layers each formed of a dielectric material having a low dielectric constant (k), and at least one load bearing support structure disposed in each of the ILD layers.

It is the Examiner's position that *Ghoshal* disclose a semiconductor device as claimed, referring specifically to ILD layers 111-121 and "support structures" 193-171 therein.

In response, it is respectfully submitted that *Goshal* does not disclose each and every limitation of the claims as required under 35 U.S.C. § 102. Instead, the claims differ structurally from *Goshal* by claiming a plurality of substantially non load bearing inter-level dielectric (ILD) layers each formed of a dielectric material having a low

dielectric constant (k), and at least one load bearing support structure disposed in each of the ILD layers.

Although the Examiner refers to elements 193-171 of *Goshal* as “support structures”, there is no disclosure to support this characterization. Instead, *Goshal* specifies that oxide island 420 performs a support function and that this oxide island necessarily includes dielectric layers to provide a support function. As stated in column 4, lines 48-40 of *Goshal*, “(t)he placement of the oxide layer is important in design because the island supports have to guarantee structural stability and be small in size”. And column 5, lines 11-13 of *Goshen* state that “selected portions of the dielectric layers (111-123) remain as dielectric supports 420 to support the interconnect islands”.

Thus, the substantially non load bearing ILD layers of the claimed invention are not taught by the *Goshal* disclosure requiring load bearing dielectric layers.

In view of the above, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 1-5, 7, 8, 10, 12, 13, 24, 25, and 27-33 under 35 U.S.C. § 102(b). Applicant further submits that claims 2-5, 7, 8, 10, 27, 28; 13, 29-30; and 25, 31-33 are in condition for allowance, at least by virtue of their dependency from allowable claims 1, 12 and 24, respectively.

Rejection of Claims 1-5, 7, 8, 10, 24-26, 30 and 31 Under 35 U.S.C. § 103(a)

In the Final Office Action, the Examiner rejected claims 1-5, 7, 8, 10, 24-26, 30 and 31 under 35 U.S.C. § 102(b) as being unpatentable over *Lin* (U.S. Patent Publication No. 2004/0253801) in view of *Peck* (U.S. Patent No. 3,427,247). This rejection is respectfully traversed.

Each of independent claims 1 and 24 is directed to a semiconductor device comprising, *inter alia*, a plurality of substantially non load bearing inter-level dielectric (ILD) layers each formed of a dielectric material having a low dielectric constant (k), and at least one load bearing support structure disposed in each of the ILD layers.

It is the Examiner's position that *Lin* discloses all elements of the claim with the exception of a dielectric material having an ultra low dielectric constant and has therefore applied *Peck* for this teaching.

To the contrary, it is respectfully submitted that *Lin* fail to disclose the claimed invention from the outset and that *Peck* fail to overcome these deficiencies. Specifically, *Lin* rely on the dielectric layers to provide support, and hence these layers are load bearing. There is no teaching or suggestion in *Lin* that at least one load bearing support structure be disposed in each of the substantially non load bearing ILD layers. It is the discovery of the present invention that the ILD layers cannot participate in load bearing when a mechanical force is applied to the semiconductor device, and further solves this problem by providing load bearing support structures in each of the ILD layers.

As described in paragraph [0062] of *Lin*, "preferably the support layer is a sacrificial dielectric layer (inter-level dielectric layer)". In distinction, the claimed invention includes a plurality of substantially non load bearing inter-level dielectric (ILD) layers, the load bearing support structure being separately provided within the substantially non load bearing ILD. With regard to an ultra-low dielectric material of *Peck*, it is respectfully submitted that this is insufficient to overcome the missing

teachings of *Lin*, and the combination therefore also fails to teach or suggest the claimed invention.

In view of the above, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 1-5, 7, 8, 10, 24-26, 30 and 31 under 35 U.S.C. § 103(a). Applicant further submits that claims 2-5, 7, 8, 10; and 25-26, 30, 31 are in condition for allowance, at least by virtue of their dependency from allowable claims 1 and 24, respectively.

CONCLUSION

Applicant respectfully requests that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing all claims into condition for allowance. Applicant submits that the proposed amendments of claims 1, 12 and 24 do not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, since all of the elements and their relationships claimed were either earlier claimed or inherent in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

Furthermore, Applicant respectfully points out that the final action by the Examiner presented some new arguments as to the application of the art against Applicant's invention. It is respectfully submitted that the entering of the Amendment would allow the Applicant to reply to the final rejections and place the application into condition for allowance.

Finally, Applicant submits that entry of the amendment would place the application into better form for Appeal, should the Examiner dispute the patentability of the pending claims.

In view of the foregoing remarks, Applicant submits that this claimed invention, as amended, is neither anticipated nor rendered obvious in view of the prior art references applied against this application. Applicant therefore requests the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

If the Examiner believes that additional discussions or information might advance the prosecution of the instant application, the Examiner is invited to contact the

undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

Please grant any extensions of time required to enter this response and charge any additional required fees to Texas Instruments' deposit account 20-0668.

Respectfully submitted,

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